REMARKS

Applicants' representative acknowledges with gratitude the courtesies extended by the Examiner during the personal interview of September 4, 2002. The present Preliminary Amendment incorporates the proposed claim amendments described in the Interview Summary.

Claims 39-51 are now pending in the present application. Claims 39, 43, and 48 have been amended by the present Preliminary Amendment as shown in Appendix A. Each of the aforementioned claims has been amended to further define the structure of the electro-mechanically polished metal layer. Support for these amendments is found in Applicants' specification at page 15, lines 10-12, (i.e., "[m]oreover the use of electrolytic techniques reduces the mechanical force required to remove metal surfaces during polishing. Finally the electrolytic bath reduces cavities or scratches in processed metal surfaces."). Aside from the disclosure of Applicants' specification, the advantages associated with the claimed electro-mechanical surface are evident from a reference disclosed in Applicants' Information Disclosure Statement filed on December 14, 2000. In the article entitled "Electrochemical Planarization for Multi-Level Metallization of Microcircuitry." Circuitree, Anthony F. Bernhardt, et al., October 1995, pp. 38-48, Figs. 3-4 illustrate the problems of utilizing a CMP polished metal layer. Figs. 9-10 of the article illustrate the benefits of utilizing an electro-mechanical polished metal layer. Particularly, Figs. 9-10 illustrate that electro-mechanically polished metal layers do not have the smearing, scratching, or deep cavities that a CMP polished metal layer possesses.

Claims 49-51 have been added to enhance the scope of protection sought to be accorded the claimed invention. Claims 49-51 define, *inter alia*, an "electro-mechanically polished noble metal surface." Support for these new claims can be found in Applicants' specification on page 7, lines 6-11. Claims 49-51 (and claims 39-48) distinguish over the Kawakubo reference cited in the Office Action of April 26, 2002. As indicated in Applicants' response of July 26, 2002, Kawakubo teaches adding an additive element such as "a solid-solution element . . . [or] a precipitation-type element" to the metal that is

utilized (Col. 6, lines 30-33). The additive increases the structural hardness and resistivity of Kawakubo's metal layer so that the metal layer can withstand CMP and MP processing (See Col. 6, lines 33-42). Applicants' claimed layer, however, is an electro-mechanically polished layer, and the noble metal does not require the use of an additive. The structure of Applicants' claimed layer, therefore, is different from that of Kawakubo.

Favorable action is respectfully solicited.

Dated: September 12, 2002

Respectfully submitted,

By_____

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APPENDIX A

39. (Amended) A semiconductor device comprising:

a substrate; and

at least one [electro-mechanical] electro-mechanically polished metal layer formed over said substrate, said electro-mechanically polished metal layer having a reduced number of cavities and/or scratches.

43. (Twice Amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an [electro-mechanical] electro-mechanically polished surface, said electro-mechanically polished surface having a reduced number of cavities and/or scratches.

48. (Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer provided over said substrate, wherein said

electro-mechanically polished layer has a reduced number of cavities and/or scratches.